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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,287	12/03/2003	Michael S. Gray	BUR920030123US1	1286

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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,287	GRAY ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/3/03,3/24/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This pertains to Application No. 10/707,287 filed 03 December 2003. Claims 1 – 20 are pending in this Application.

Claim Objection

2. Claims 5, 12 and 17 are objected to because of the following informalities: it is unclear what is meant by the phrase "longest path algorithm cannot be completed due to ***a positive cycle.***" More details on the meaning of a positive cycle are needed. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1 – 7, 9 – 12 and 14 – 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Publication No. US 2005/0060672 A1 to Poechmueller.

5. Referring to claims 1, 10 and 15, Poechmueller discloses a method (claim 1), a system (claim 10 – see Fig. 5; page 5, paragraph 0052), and a computer program (claim 15 – see Fig. 5; page 5, paragraph 0053) for minimizing area of a circuit design (see page 1, paragraphs 0001 and 0002) comprising: (a) applying a longest path algorithm to the circuit design to determine a minimum legal size (see Fig. 3;

paragraphs 0032 – 0037); (b) calculating a scaling factor based on the ratio of the minimum legal size divided by a pre-compaction size (see Fig. 3, steps 12 and 13; paragraphs 0012, 0013; paragraphs 0030, 9931, 0043 – 0046, which collectively cite using a "scaling factor" to increase/decrease spacing, predetermined according to block size); and (c) scaling the circuit design using the scaling factor while maintaining an objective (see again Fig. 3; paragraph 0044). Thus, Poechmueller teaches the claimed limitations.

6. As per claim 2, see paragraphs 0006 and 0007, which recite how the size is measured from a boundary (an edge of the layout) to an opposite boundary (another edge of the layout), as claimed.

7. Regarding claim 3, see paragraphs 0036 and 0037, which cite the step of fixing an element size before applying the scaling and longest path algorithm steps.

8. As for claim 4, see paragraph 0007, which cites assigning a sink (i.e., top edge) and a source (i.e., bottom edge) as claimed.

9. As to claim 5, see paragraphs 0013 and 0041, which teach how certain design constraints can be ignored in certain cases (i.e., when the longest path algorithm cannot be completed).

10. Referring to claim 6, see also paragraph 0005 which recites how the element size is fixed prior to scaling as claimed.

11. As for claim 7, see paragraphs 0004 and 0036, which cite how elements include a device and a wire as claimed.

12. Regarding claim 9, see paragraphs 0028, 0029, and 0037, which teach the claimed limitation pertaining to the objective that include distance between elements and relative position between elements.

13. Claims 11, 12 and 14 contain the same limitations found in claims 2, 5 and 6, respectively, and thus the same rejections also apply.

14. Claims 16, 17 and 18 contain the same limitations as in claims 4, 5 and 6 respectively, and therefore the same rejections apply.

15. Claim 19 contains the same limitations found in claims 3 and 6, and thus the same rejections also apply.

Claim Rejections - 35 USC § 103

16. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 8, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poechmueller in view of "A VLSI Artwork Legalization Technique Based on a New Criterion of Minimum Layout Perturbation " (Proceedings of the 1997 International Symposium on Physical Design, pp. 116 – 121) to Heng et al. (hereinafter "Heng").

18. Poechmueller teaches a method, a system and a computer program for minimizing area of a circuit using a longest path algorithm and a scaling factor, as cited above. But Poechmueller does not teach applying a minimum perturbation analysis to the scaled circuit design to correct ground rule error to the scaled circuit design. But

Heng in fact teaches the limitation of the minimum layout perturbation analysis to correct VLSI layouts (see Abstract; Introduction and Motivation on page 116). Furthermore, Heng provides a good motivation for combining both inventions: as more advanced technologies become available, existing physical layout is mapped or scaled to new technology to boost performance, requiring adjustments to maintain design rule correctness of the layout, which can require a lot of resources and layout technicians to accomplish; whereby minimum perturbation analysis will cure this deficiency, which also applies to scaling down a circuit layout (see Heng - Motivation on page 116). Therefore it would be obvious to a person of ordinary skill in art at the time the invention was made to combine Poechmueller and Heng to obtain a way to ***minimize the area*** of a circuit design using a method that will ***minimally perturb*** the layout, in order to ***save time*** and ***human resources*** (cited by Heng on page 116, Section 2).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
06 February 2006

MYD

JACK CHIANG
SUPERVISORY PATENT EXAMINER